AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An error correction method for performing error correction on data which are interleaved and ~~are~~ composed of ~~plural~~ code lines, said method comprising:

a step of giving ~~parameters~~ erasure position information for tracking down errors in the respective code lines;

a rearrangement step of rearranging the code lines in the order in which error correction is to be carried out;

a judgement step of, with a code line to be subjected to error correction being in a target code line, ~~comparing the parameter~~ judging whether or not the position of the target byte in said target code line ~~that is given in the step of giving the parameters, with the parameter~~ is on the boundary with a data region which comprise error correction codes that are independent from error correction codes in said target code line, with the erasure position information which is used when performing error correction on a code line that is previous to the target code line in the error correction order, and judging, according to the result of ~~the comparison~~ judgement, as to which ~~parameter is~~ erasure position information to be used for tracking down an error in the target block, the ~~parameter~~ erasure position information in the target code line or the ~~parameter~~ erasure position information which is used when performing error correction on the code line that is previous to the target code line in the error correction order; and

an error correction step of performing error correction on the data for every code line, using the ~~parameter~~ erasure position information.

2. (Currently Amended) An error correction method as defined in Claim 1, wherein the ~~parameter~~ erasure position information for tracking down an error in the target code line is determined before performing an error correction on the target code line.

3. (Currently Amended) An error correction method as defined in Claim 1, wherein[[,]] in said rearrangement step, the order of the code lines of the data are rearranged at intervals of at least two lines.

4. (Currently Amended) An error correction method as defined in Claim 1, further including a first error correction incapability judgement step of judging whether or not the target code line is incapable of being subjected to error ~~correction,~~ correction on the basis of the ~~parameter~~ erasure position information;

wherein error correction is carried out without using the ~~parameter~~ erasure position information when the result of the judgement in the first error correction incapability judgement step indicates [["]]incapable of error correction[["]].

5. (Currently Amended) An error correction method as defined in Claim 4, further including a second error correction incapability judgement step of judging whether or not a code line that is previous to the target code line in the error correction order was incapable of being subjected to error correction;

wherein the target code line is subjected to error correction using the ~~parameter~~ erasure position information of the target code line when the result of the judgement in the second error correction incapability judgement step indicates [["]]incapable of error correction[["]].

6. (Currently Amended) An error correction method as defined in Claim 1_a wherein said data are stored in an optical medium.

7. (Currently Amended) An error correction apparatus for performing error correction on data which are interleaved and are composed of plural code lines, said apparatus comprising:

a first memory circuit for storing data to be subjected to error correction;

a first control circuit for performing control so as to rearrange data being transferred from the first memory circuit to the error correction circuit, in the order in which the data are to be subjected to error correction;

an error correction circuit for performing error correction on the data stored in the first memory circuit, for each code line, using ~~parameters~~ erasure position information for tracking down errors in the code lines;

a storage unit for storing ~~parameters~~ erasure position information that have been used for error correction by the error correction circuit;

a comparator for comparing the ~~parameter~~ erasure position information of the target code line with the ~~parameter~~ erasure position information which has been used when performing error

correction on a code line that is previous to the target code line in the error correction order and is stored in the storage unit;

wherein said control circuit rearranges the order of the code lines to be subjected to error correction, at intervals of at least two code lines; and

said error correction circuit performs error correction on the target code line, according to the result of the comparison by the comparator, using, as the ~~parameter~~ erasure position information for tracking down an error in the target code line, the parameter of the target code line or the ~~parameter~~ erasure position information which has been used when performing error correction on a code line that is previous to the target code line in the error correction order.

8. (Currently Amended) An error correction apparatus as defined in Claim 7, further including:

a second memory circuit for storing the ~~parameters~~ erasure position information; and

a second control circuit for performing control so as to read the ~~parameters~~ erasure position information from the second memory circuit, and transferring the ~~parameters~~ erasure position information.

9. (Currently Amended) An error correction apparatus as defined in Claim 7, wherein said storage unit is provided with a group of registers.

10. (Currently Amended) An error correction apparatus as defined in Claim 9, wherein said group of registers hold the ~~parameters~~ erasure position information which ~~are~~ is obtained from the second memory circuit through the second control circuit.

11. (Currently Amended) An error correction apparatus as defined in Claim 10, wherein said group of registers includes:

a first register for holding the number of ~~parameters~~ the erasure position information obtained from the second memory circuit; and

a second register for holding the ~~parameters~~ erasure position information obtained from the second memory circuit.

12. (Currently Amended) An error correction apparatus as defined in Claim 11, wherein said second register is a shift register.

13. (Currently Amended) An error correction apparatus as defined in Claim 8, wherein said second control circuit generates addresses to be used when reading ~~the parameters from the second memory circuit on the basis of the information~~ said erasure position information stored in the group of registers.

14. (Currently Amended) An error correction apparatus as defined in Claim 8, wherein said data comparator compares the ~~parameters~~ erasure position information stored in the second memory circuit with the ~~parameters~~ erasure position information stored in the second register.

15. (Currently Amended) An error correction apparatus as defined in Claim 7, wherein said first control circuit performs control such that at least two code lines of data to be subjected to error correction are simultaneously transferred from the first memory circuit to the error correction circuit; and

said error correction circuit has a means capable of receiving at least two code lines of data simultaneously.

16. (Currently Amended) An error correction apparatus as defined in Claim 7, wherein said data are stored in an optical medium.

17. (New) An error correction method for using sub data which comprise error correction codes that are independent from error correction codes of code line in error correction target to configure erasure position information, said method comprising:

a judgment step for judging whether or not a first data, which is one of the elements of code line in said error correction target, and a second data, which exists on the same position as the first data in the code line of previous error correction, existed between the same sub data before being deinterleaved;

a configuration step for configuring erasure position information of said second data as erasure position information of said first data when the first and second data existed between the same sub data; and

an error correction step for performing error correction on the code line in said error correction target.

18. (New) An error correction method as defined in Claim 17, wherein said code line in error correction target extends between plural of sub data before being deinterleaved.

19. (New) An error correction method as defined in Claim 17, wherein the method uses sync data which is inserted between data at predetermined intervals to configure the erasure position information of said first data.

20. (New) An error correction method as defined in Claim 19, wherein said judgment step judges the first data does not exist between the same sub groups with said second data when said first data is the next data to a sub data region or a sync region of the data recording order.

21. (New) An error correction method as defined in Claim 20, wherein an error correcting step performs error correction without using said erasure position information when the number of erasure position information configured in said configuring step is higher than the number of parity data.

22. (New) An error correction method for using sub data which comprises error correction codes that are independent from error correction codes of code line in error correction target to configure erasure position information, said method comprising:

a judgment step for judging whether or not a first data, which is one of the elements of code line in said error correction target, and a second data, which exists on the same position as the first data in the code line of previous error correction, existed between the same sub data before being deinterleaved when the code line of the previous error correction performed error correction by using said erasure position information;

a configuration step for configuring erasure position information of said second data as erasure position information of said first data when said judgment step judges the first and second data existed between the same sub data, and configuring every element of code line in said error correction target when the code line of the previous error correction performed error correction without using erasure position information; and

an error correction step for performing error correction on the code line in said error correction target.

23. (New) An error correction method as defined in Claim 22, wherein said code line in error correction target extends between plural of sub data.

24. (New) An error correction method as defined in Claim 22, wherein the method uses sync data which is inserted between data at predetermined intervals to configure the erasure position information of said first data.

25. (New) An error correction method as defined in Claim 24, wherein said judgment step judges the first data do not exist between the same sub groups with said second data when said first data is the next data to a sub data region or a sync region of the data recording order.

26. (New) An error correction method as defined in Claim 25, wherein said error correction step performs error correction without using said erasure position information when the number of erasure position information configured in said configuration step is higher than the number of parity data.

27. (New) An error correction apparatus using sub data which comprises error correction codes that are independent from error correction codes of code line in error correction target to configure erasure position information, said apparatus comprising:

a judgment means for judging whether or not a first data, which is one of the elements of code line in said error correction target, and a second data, which exist on the same position as the first data in the code line of previous error correction, existed between the same sub data before being deinterleaved;

a configuration means for configuring erasure position information of said second data as erasure position information of said first data when the first and second data existed between the same sub data; and

an error correction means for performing error correction on the code line in said error correction target.

28. (New) An error correction apparatus as defined in Claim 27, wherein said code line in error correction target extends between plural of sub data before being deinterleaved.

29. (New) An error correction apparatus as defined in Claim 27, wherein the apparatus uses sync data which is inserted between data at predetermined intervals to configure erasure position information of said first data.

30. (New) An error correction apparatus as defined in Claim 29, wherein said judgment means judges said first data does not exist between the same sub groups with said second data when said first data is the next data to a sub data region or a sync region of the data recording order.

31. (New) An error correction apparatus as defined in Claim 30, wherein said error correction means performs error correction without using said erasure position information when

the number of said erasure position information configured by said configuration means is higher than the number of parity data.

32. (New) An error correction apparatus using sub data which comprises error correction codes that are independent from error correction codes of code line in error correction target to configure erasure position information, said apparatus comprising:

a judgment means for judging whether or not a first data, which is one of the elements of code line in said error correction target, and a second data, which exists on the same position as the first data in the code line of previous error correction, existed between the same sub data before being deinterleaved when the code line of the previous error correction performed error correction by using said erasure position information;

a configuration means for configuring erasure position information of said second data as erasure position information of said first data when said judgment step judges the first and second data existed between the same sub data, and configuring every element of code line in said error correction target when the code line of the previous error correction performed error correction without using erasure position information; and

an error correction means for performing error correction on the code line in said error correction target.

33. (New) An error correction apparatus defined in Claim 32, wherein said code line in error correction target extends between plural of sub data before being deinterleaved.

34. (New) An error correction apparatus defined in Claim 32, wherein the apparatus uses sync data which is inserted between data at predetermined intervals to configure erasure position information of said first data.

35. (New) An error correction apparatus defined in Claim 34, wherein said judgment means judges said first data does not exist between the same sub groups with said second data when said first data is the next data to a sub data region or a sync region of the data recording order.

36. (New) An error correction apparatus defined in Claim 35, wherein said error correction means performs error correction without using said erasure position information when the number of erasure position information configured in said configuration means is higher than the number of parity data.

37. (New) An error correction method as defined in Claim 18, wherein the method uses sync data which is inserted between data at predetermined intervals to configure the erasure position information of said first data.

38. (New) An error correction method as defined in Claim 23, wherein the method uses sync data which is inserted between data at predetermined intervals to configure the erasure position information of said first data.

39. (New) An error correction apparatus as defined in Claim 28, wherein the apparatus uses sync data which is inserted between data at predetermined intervals to configure erasure position information of said first data.

40. (New) An error correction apparatus defined in Claim 33, wherein the apparatus uses sync data which is inserted between data at predetermined intervals to configure erasure position information of said first data.